	Туре	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1553	(ruthenium or Ru) near4 (gas or precursor or reactant)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:18
2	BRS	L2	1735	(ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:18
3	BRS	<b>L3</b>	3535	adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	1
4	BRS	L4	266646	"O.sub.2" or "N.sub.20" or "H.sub.20" or "NO.sub.2" or "O.sub.3"		2004/10/13

	Туре	L #	Hits	Search Text	DBs	Time Stamp
5	BRS	<b>L</b> 5	51	or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or	DERWEN T; IBM_TD B	

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	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6		ethylcyclopentadiencyl) or	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:18
7	BRS	L7	661200		USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:18

	Туре	L #	Hits	Search Text	DBs	Time Stamp
8	BRS	L8	5188	<pre>((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.2H.sub.190.sub.2") )))</pre>	US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:18
9	BRS	L9	125468 3	("O.sub.2" or "N.sub.20" or "H.sub.20" or "NO.sub.2" or "O.sub.3") or (oxygen or oxidiz\$4 or oxidat\$4)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19

	Type	L #	Hits	Search Text	DBs	Time	Stamp
10	BRS	L10	331	cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/ 12:19	

	Туре	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	<b>L11</b>	838	cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19

	Туре	L #	Hits	Search Text	DBs	Time Stamp
12	BRS	L12	5188	<pre>((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.22H.sub.190.sub.2") )))</pre>	US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19
13	BRS	L13	125468 3	("O.sub.2" or "N.sub.20" or "H.sub.20" or "NO.sub.2" or "O.sub.3") or (oxygen or	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19

	Туре	L #	Hits	Search Text	DBs	Time Stamp
14	BRS	<b>L14</b>		(((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadienyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.2H.sub.19O.sub.2") )))) near8 (absorp\$6 or adsorb\$6) near8 (("O.sub.2" or "N.sub.20" or "H.sub.20" or "No.sub.2" or "O.sub.3") or (oxygen or oxidiz\$4 or oxidat\$4))	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13

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(((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadienyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj or (bis adj ethylcyclopentadienyl) or (tris adj dipivaloylmethanate) or (Ru near2  (((ruthenium or Ru) near4 (gas or precursor or (ruthenium or Ru USPAT; US-PGP UB; EPO; JPO; DERWEN 12:19		Туре	L #	Hits	Search Text	DBs	Time	Stamp
("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.22H.sub.19O.sub.2") )))) near8 (stop\$4 or terminat\$4 or end\$4 or reduc\$4 or slow\$4 or paus\$4 or cycl\$4 or puls\$4)	15	BRS	L15		(gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadienyl or bis-ethylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("Ch.sub.2H.sub.5C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.19O.sub.2"))))) near8 (stop\$4 or terminat\$4 or end\$4 or reduc\$4 or slow\$4	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	12:19	

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-	Туре	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	69	ethylcyclopentadiencyl) or	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19

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	Туре	L #	Hits	Search Text	DBs	Time	Stamp
17	BRS	L17		or bis-ethylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/ 12:19	

	Type	L #	Hits	Search Text	DBs	Time Stamp
18	BRS	L18	358		US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19

	Туре	L #	Hits	Search Text	DBs	Time Stamp
19	BRS	L19		(((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.22H.sub.19O.sub.2") )))) near8 ("H.sub.2" or hydrogen) near8 (anneal\$4 or reduc\$4)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:19

	Туре	L #	Hits	Search Text	DBs	Time S	Stamp
20	BRS	L20	48	dipivaloyimethanate) or (Ru near2 ("CH sub 3C sub 54 sub 44))	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/1 12:19	0/13

	Туре	L #	Hits	Search Text	DBs	Time Stamp
21	BRS	L22	1026	<pre>adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or</pre>	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20

	Туре	L #	Hits	Search Text	DBs	Time Stamp
22	BRS	L23	101	adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2	В	

	Туре	L #	Hits	Search Text	DBs	Time Stamp
23	BRS	L24	838	or bis-ethylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20

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	Туре	L #	Hits	Search Text	DBs	Time St	amp
24	BRS	L25		cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/ 12:20	13

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	Type	L #	Hits	Search Text	DBs	Time Stamp
25	BRS	L26	157	((((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadienyl or bis-ethylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadienyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.2H.sub.190.sub.2") )))) same ("O.sub.2" or "N.sub.20" or "H.sub.20" or "N.sub.20" or "O.sub.3")) and ((capacitor\$3 or DRAM or (dynamic adj random adj access adj memory) or SDRAM))	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20

	Туре	L #	Hits	Search Text	DBs	Time Stamp
26	BRS	L27	18	(((((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadienyl or bis-ethylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadiencyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.2H.sub.19O.sub.2") )))) same ("O.sub.2" or "N.sub.20" or "H.sub.20" or "N.sub.20" or "O.sub.3")) and ((capacitor\$3 or DRAM or (dynamic adj random adj access adj memory) or SDRAM))) and @py<2001	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20

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	Туре	L #	Hits	Search Text	DBs	Time Stamp
27	BRS	L28	36	ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4"))	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20

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	Туре	L #	Hits	Search Text	DBs	Time Stamp
28	BRS	L30	430	(((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas\$3 or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or bis-methylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadiencyl) or (bis adj ethylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.su b.4")) or (Ru near2 ("C.sub.22H.sub.19O.sub.2") )))) near8 (("O.sub.2" or "N.sub.20" or "H.sub.20" or "NO.sub.2" or "O.sub.3") or (oxygen or oxidiz\$4 or oxidat\$4))	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20
29	IS&R	L31	2	("6297122").PN.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13
30	IS&R	L32	2	("6617248").PN.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:20

	Туре	L #	Hits	Search Text	DBs	Time Stamp
31	BRS	L33		((((ruthenium or Ru) near4 (gas or precursor or reactant)) or ((ruthenium or Ru) near4 (gas or precursor\$3 or reactant\$3)) or ((bis-cyclopentadienyl or (bis-methylcyclopentadienyl or bis-methylcyclopentadiencyl or tris-dipivaloylmethanate or (bis adj cyclopentadienyl) or (bis adj methylcyclopentadiencyl) or (bis adj methylcyclopentadiencyl) or (tris adj dipivaloylmethanate) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("CH.sub.3C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.5C.sub.5H.sub.4")) or (Ru near2 ("C.sub.2H.sub.190.sub.2") )))) near8 (stop\$4 or terminat\$4 or end\$4 or reduc\$4 or slow\$4 or paus\$4 or cycl\$4 or puls\$4)) same (("O.sub.2" or "N.sub.20" or "H.sub.20" or "NO.sub.2"	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:36
32	BRS	L34	665		USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:36
33	BRS	<b>L35</b>	466	34 and ((@ad<20010131) or (@rlad<20010131))	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/10/13 12:37

DOCUMENT-IDENTIFIER:

US 20010031527 A1

TITLE:

Semiconductor memory device

incorporating therein

ruthenium electrode and method for

the manufacture

thereof

----- KWIC -----

Pre-Grant Publication Year - PGPY (1):
 2001

Summary of Invention Paragraph - BSTX (4):

[0002] As is well known, a  $\underline{\text{dynamic random access memory}}$  (DRAM) with at least

one memory cell comprised of a transistor and a capacitor has a higher degree

of integration mainly by down-sizing through micronization. However, there is

still a demand for downsizing the area of the memory cell.

Summary of Invention Paragraph - BSTX (5):

[0003] To meet the demand, therefore, there have been proposed several

methods, such as a trench type or a stack type capacitor,
which is arranged

three-dimensionally in a memory device to reduce the cell area available to the

capacitor. However, the process of manufacturing
three-dimensionally arranged

capacitor is a long and tedious one and consequently
involves high

manufacturing cost. Therefore, there is a strong demand for a new memory

device that can reduce the cell area with securing a requisite volume of

information without requiring complex manufacturing steps.

Summary of Invention Paragraph - BSTX (6): [0004] In attempt to meet the demand, **DRAM** device

employs a high dielectric

material as a <u>capacitor</u> thin film such as barium strontium titanate (BST) and

tantalum oxide (Ta.sub.20.sub.5). Meanwhile, ferroelectric random access

memory (FeRAM) employs a ferroelectric material as a capacitor thin film such

as strontium bithmuth tantalate (SBT) and lead zirconate titanate (PZT) in

place of a conventional silicon oxide film or a silicon nitride film.

Summary of Invention Paragraph - BSTX (7):

[0005] However, even if the high dielectric material is used as the

<u>capacitor</u> thin film, it has still a problem that an increase of a capacitance

has a limitation by using a conventional method for forming the stack or the

trench capacitor structure.

Detail Description Paragraph - DETX (2):

[0015] There are provided in FIGS. 1 and 2A to 2C a cross sectional view of

a semiconductor device 100 incorporated therein a trench type **capacitor** and

cross sectional views setting forth a method for the manufacture thereof in

accordance with a preferred embodiment of the present invention. It should be

noted that like parts appearing in FIGS. 1 and 2A to 2C are represented by like reference numerals.

Detail Description Paragraph - DETX (9):

[0022] In a next step as shown in FIG. 2C, a second Ru layer 132 with a

rough surface is formed on the first Ru layer 130 by using a thermal chemical

vapor deposition (TCVD) technique, thereby obtaining a Ru electrode structure

140. Like a conventional hemispherical grain silicon (HSGs), the second  ${\tt Ru}$ 

layer 132 has a rugged surface of hemispherical grain so that a surface area of

the electrode increases and a capacitance increases. Here, the TCVD is

performed on a condition that used gas is Ru

(C.sub.5H.sub.5).sub.2/0.sub.2, a

temperature ranges from approximately 200 to approximately 400 and a pressure

ranges from approximately 40 mTorr to approximately 200 mTorr. In order to

form the rugged surface of the second Ru layer 132, the deposition temperature

should be low because it is difficult to grow up nuclei of the Ru at the low

temperature. Additionally, roughness of the Ru surface is varied by means of

oxygen content in the second Ru layer 132.

Detail Description Paragraph - DETX (10):

[0023] Referring to FIGS. 3 and 4A to 4D, there are provided cross sectional

view of a semiconductor device 200 incorporated therein a stack type capacitor

and cross sectional views setting forth a method for the manufacture thereof in

accordance with another preferred embodiment of the present invention. It

should be noted that like parts appearing in FIGS. 3 and 4A to 4D are

represented by like reference numerals.

Detail Description Paragraph - DETX (18):

[0031] Finally, a second Ru layer 232 with a rough surface is formed on the

patterned Ru layer 230A by using a thermal chemical vapor deposition (TCVD)

technique, thereby obtaining a Ru electrode structure 240 as shown in FIG. 4D.

The TCVD is performed on a condition that used **gas is Ru**(C.sub.5H.sub.5).sub.2/O.sub.2, a temperature ranges from approximately 200

to approximately 400 and a pressure ranges from approximately 40 mTorr to

approximately 200 mTorr. In order to form the rugged surface of the second Ru

layer 232, the deposition temperature should be low because it is difficult to

grow up nuclei of the Ru at the low temperature.

Claims Text - CLTX (6):

5. The semiconductor device as recited in claim 1, wherein a <u>capacitor</u> structure of the semiconductor device is a trench type.

Claims Text - CLTX (7):

6. The semiconductor device as recited in claim 1, wherein a <u>capacitor</u> structure of the semiconductor device is a stack type.

Claims Text - CLTX (12):

11. The method as recited in claim 7, wherein the step c) is carried using a gas of Ru(C.sub.5H.sub.5).sub.2/0.sub.2.

Claims Text - CLTX (14):

13. The method as recited in claim 7, wherein a capacitor structure of the semiconductor device is a trench type.

Claims Text - CLTX (15):

14. The method as recited in claim 7, wherein a capacitor structure of the semiconductor device is a stack type.

US-PAT-NO:

6287934

DOCUMENT-IDENTIFIER:

US 6287934 B1

TITLE:

Capacitor structure of semiconductor

memory cell and

method for fabricating capacitor

structure of

semiconductor cell

----- KWIC -----

Abstract Text - ABTX (1):

A <u>capacitor</u> structure in a semiconductor memory cell includes a lower

electrode formed on a base body, a capacitor insulation film which is a

ferroelectric thin film formed on the lower electrode, and an upper electrode

formed on the <u>capacitor</u> insulation film. The lower electrode is shaped

semi-spherical. The  $\underline{\text{capacitor}}$  structure has an increased area of the upper

electrode in contact with the ferroelectric thin film, local concentration of

an electric field in the ferroelectric thin film is unlikely to occur.

TITLE - TI (1):

<u>Capacitor</u> structure of semiconductor memory cell and method for fabricating <u>capacitor</u> structure of semiconductor cell

YEAR ISSUED - PY (1): 2001

Brief Summary Text - BSTX (3):

This invention relates to a <u>capacitor</u> structure in a semiconductor memory cell using a ferroelectric thin film and a method for fabricating such a

electrode layer, and a
capacitor insulation film made of the ferroelectric film;
and

Brief Summary Text - BSTX (38):

In the method for fabricating a capacitor structure in a semiconductor memory cell according to the third or fourth aspect of the invention, in the step (a) of forming the base layer, an upper portion of the base body not covered by the base layer is preferably removed. It leads to a more increase in the capacitor effective area, and hence a more increase in the amount of stored charge. The base layer may be an insulation material layer or a conductive material layer. If the base layer is a conduction material layer,

it may be a barrier metal layer, or may be an upper end of a contact plug extending from a source/drain region of a select transistor formed under the

capacitor structure.

Usable for making the

Brief Summary Text - BSTX (44):

The lower electrode (lower electrode layer) and/or the upper electrode (electrode thin film) in the capacitor structure of the semiconductor memory cell according to the invention may be made of, for example, RuC.sub.2, IrO.sub.2, layered RuO.sub.2 /Ru, Pt, Pd, layered Pt/Ti, layered of Pt/Ta, layered Pt/TiTa, La.sub.0.5 Sr.sub.0.5 CoO.sub.3 (LSCO), layered Pt/LSCO, or YBa.sub.2 Cu.sub.3 O.sub.7. In multi-layered films shown above, materials appearing left of "/" form a layer adjacent the ferroelectric thin film whereas materials appearing right of "/" form a layer adjacent the base body or a plate line. The upper electrode may commonly form the plate line, or a separate plate line other than the upper electrode may be formed.

upper electrode layer and the electrode thin film are sputtering or pulse laser ablation. Usable for patterning the lower electrode layer and the electrode thin film is, for example, ion milling or RIE.

Brief Summary Text - BSTX (46):

the invention:

The semiconductor memory cell having the <u>capacitor</u> structure according to the invention may be a nonvolatile memory cell (so-called FERAM) or <u>DRAM</u>.

Drawing Description Text - DRTX (5):
FIG. 4 is a schematic fragmentary cross-sectional view of a <u>capacitor</u>
structure in a semiconductor memory cell according to the first embodiment of

Drawing Description Text - DRTX (6):
FIGS. 5A and 5B are schematic fragmentary
cross-sectional views of a
semiconductor substrate and other elements for explaining a
method for
fabricating a <u>capacitor</u> structure of a semiconductor memory
cell according to
the first embodiment of the invention;

Drawing Description Text - DRTX (7):

FIGS. 6A and 6B are schematic fragmentary
cross-sectional views of the
semiconductor substrate and other elements for explaining
the method for
fabricating the <u>capacitor</u> structure of the semiconductor
memory cell,
subsequent to FIGS. 5A and 5B;

Drawing Description Text - DRTX (8):

FIG. 7 is a schematic fragmentary cross-sectional view of a capacitor structure of a semiconductor memory cell as a modified version of the first embodiment;

Drawing Description Text - DRTX (9):

FIG. 8 is a schematic fragmentary cross-sectional view of a semi-processed

configuration of a **capacitor** structure of a semiconductor memory cell according

to the first embodiment of the invention;

Drawing Description Text - DRTX (10):

FIG. 9 is a schematic fragmentary cross-sectional view of the <u>capacitor</u>

structure of the semiconductor memory cell according to the second embodiment of the invention;

Drawing Description Text - DRTX (11):

FIG. 10 is a schematic fragmentary cross-sectional view of a capacitor

structure of a semiconductor memory cell according to the fourth embodiment of the invention;

Drawing Description Text - DRTX (12):

FIG. 11 is a schematic fragmentary cross-sectional view of the  ${\color{red} {\bf capacitor}}$ 

structure of the semiconductor memory cell according to the fourth embodiment of the invention;

Drawing Description Text - DRTX (13):

FIG. 12 is a schematic fragmentary cross-sectional view of a  ${\color{blue}{\bf capacitor}}$ 

structure of a semiconductor memory cell according to the fifth embodiment of the invention;

Drawing Description Text - DRTX (14):

FIG. 13 is a schematic fragmentary cross-sectional view of a **capacitor** 

structure of a semiconductor memory cell according to the sixth embodiment of the invention;

Detailed Description Text - DETX (53):

Subsequently, DC sputtering is performed using Ru (ruthenium) as the and

O.sub.2 /Ar as the process gas to form the lower electrode layer 21A made of

RuO.sub.2 on the entire surface involving the insulation material layer 40.

The lower electrode layer 21A is then dry-etched by RIE using O.sub.2

/Cl.sub.2. In this manner, the semi-spherical insulation material layer 40

made of SiN, and the lower electrode made of the lower electrode layer 21A

stacked on the insulation material layer 40, can be obtained. Note here that

dry-etching of the lower electrode layer 21A is conducted for patterning the

lower electrode layer 21A, and not for shaping the lower electrode layer 21

semi-spherical. The surface of the lower electrode layer 21A on which the

ferroelectric thin film should be made is covered by the resist material during

etching of the lower electrode layer 21A. Therefore, the ferroelectric thin

film can be formed on the lower electrode layer 21A maintaining its original

surface condition, and deterioration in P-E hysteresis loop characteristics of

the ferroelectric thin film can be prevented.

Detailed Description Text - DETX (54):

The structure of the lower electrode explained with the fifth embodiment is

applicable to the lower electrode of the capacitor
structure of the

semiconductor memory explained with either the second or fourth embodiment.

Moreover, the method for fabricating the **capacitor** structure of the

semiconductor memory cell explained with the third embodiment can be used for

fabricating the lower electrode structure explained with the fifth embodiment.

Additionally, a barrier metal layer may be formed between the lower electrode

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TITLE:

Methods for preparing ruthenium

oxide films

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Brief Summary Text - BSTX (5):

Thus, films of ruthenium and oxides thereof have suitable properties for a

variety of uses in integrated circuits. For example, they can be used in

integrated circuits for electrical contacts. They are particularly suitable

for use as barrier layers between the dielectric material and the silicon

substrate in memory devices, such as ferroelectric memories. Furthermore, they

may even be suitable as the plate (i.e., electrode) itself in capacitors.

Detailed Description Text - DETX (7):

The precursor composition can be vaporized in the presence of one or more  $% \left( 1\right) =\left( 1\right) \left( 1\right) +\left( 1\right) \left( 1\right) \left( 1\right) +\left( 1\right) \left( 1\right$ 

reaction gases and optionally one or more inert carrier gases to form a

ruthenium oxide film. The inert carrier gas is typically selected from the

group consisting of nitrogen, helium, argon, and mixtures thereof. In the

context of the present invention, an inert carrier gas is one that is generally

unreactive with the complexes described herein and does not interfere with the

formation of a ruthenium oxide film. The reaction gas can be selected from a

wide variety of oxidizing gases reactive with the complexes

described herein,

at least at a surface under the conditions of chemical vapor deposition.

Examples of oxidizing gases include <a>O.sub.2</a>, <a>N.sub.2</a> o, <a>O.sub.3</a>, <a>NO</a>, <a>NO.sub.2</a>,

H.sub.2 O.sub.2, and H.sub.2 O. Various combinations of reaction gases and

optional carrier gases can be used in the methods of the present invention to form films.

Detailed Description Text - DETX (18):

The use of the complexes and methods of forming films of the present

invention are beneficial for a wide variety of thin film applications in

semiconductor structures, particularly those requiring diffusion barriers. For

example, such applications include <u>capacitors</u> and metallization layers, such as

multilevel interconnects in an integrated circuit structure. Such structures

are described, for example, in Applicants' Assignees' copending patent

application entitled "Ruthenium Silicide Diffusion Barrier Layers and Methods

of Forming Same, "having Ser. No. 09/141,240, dated Aug. 27, 1998, and filed

on even date herewith now U.S. Pat. No. 6,197,628.